REMARKS

Applicants have carefully reviewed the Office Action dated November 12, 2004. Claims 1-6 and 8-13 are pending in this application. Claims 1-6 remain for examination and Claims 8-13 remain withdrawn. Applicants have amended Claim 1 to more clearly point out the present inventive concept. Reconsideration and favorable action is respectfully requested.

Claims 1-6 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The Examiner has specifically referred to the language "the functionality associated therewith" in Claim 1. This has been amended, but Applicants note that this language refers to the fact that the reconfigurable interface defines both how the plurality of input/output pins interface with select ones of the plurality of function blocks and also defines the associated functionality. Applicants have amended this to more clearly point this out. Therefore, Applicants believe that, as amended, Claim 1 now overcomes the 35 U.S.C. §112 rejection, the withdrawal of which is respectfully requested. The withdrawal of the 35 U.S.C. §112 rejection with respect to Claims 5-6, dependent from Claim 1, is also respectfully requested.

Claims 1-6 stand rejected under 35 U.S.C. §103(a) as being obvious in view of the combination of *Cheung et al.* and *Allen et al.*, both discussed in previous Office Actions.

The *Cheung et al.* reference discloses a reconfigurable circuit that provides a plurality of functional modules, specifically illustrated in Figure 2a, that have a crossbar switch for interfacing those functional modules to a plurality of input/output pins. An external memory is required to configure this module for the various pin output configurations. There is no processor provided on board; rather, the only one chip processor is that illustrated in the prior art version of Figure 1a which does not include the reconfigurable interface as set forth in the present claims that is associated with an on-chip memory. Thus, the integrated circuit that is disclosed in *Cheung et al.* has only the functional modules, and the crossbar switch which is configurable, but the configuration must be provided by external memory.

The *Allen et al.* reference has been provided by the Examiner to cure one deficiency in the

teaching of *Cheung et al.*, that teaching being the I/O pin configuration stored in memory that is on-chip and non-volatile. The *Allen et al.* reference illustrates an on-board processor and an on-board non-volatile memory in the form of an EPROM. There is provided the ability to interface the processor with two configurable pins. This allows an output of the CPU to be routed to one of two pins and/or an input of the CPU to be connected to one of two pins. Thus, in one mode of operation, two inputs to the CPU could be received from two different pins, in another mode, one input and one output provided, and in yet another mode two outputs provided. The inputs/outputs can be routed to any of the two pins and this configuration is provided in the on-board memory. However, there is no functional input/output module that allows the processing core to interface with the plurality of input/output pins wherein the interface both defines which input/output pin the functional block is connected to and also defines the associated functionality. In *Allen et al.*, it can be seen that the only functionality associated with a particular pin is associated with that pin permanently. For example, the microprocessor can be interfaced with the pin through the buffers for (411) and (412), but these are always associated with that pin. Thus, there must be two buffers provided for two pins. This is different than Applicants' present inventive concept, wherein the functional blocks have the output thereof routed to different pins, and which functional blocks provide an interface between the processor core and the input/output pins. There is no functional block illustrated in *Allen et al.* that has the output thereof routed to two different pins. These functional blocks as set forth in the amended claims comprise input/output functional blocks that allow the processing core to interface with the input/output pins. As such, there is no suggestion in *Allen et al.* to provide a functional input/output pin that interfaces between a processing core and external input/output pins in such a manner that there could be a plurality of functional blocks with outputs that exceed the number of input/output pins and wherein an on-chip memory can define the configuration that selects which of the functional blocks are provided for the input/output interface between the processing core and select ones of the pins. Therefore, Applicants believe that there is no motivation for the combination of *Allen et al.* and *Cheung et al.* for the purpose of providing an on-chip microprocessor core, the plurality of functional input/output blocks that allow the processor core to interface with select ones of the input/output pins, which selection of functional blocks and pin configuration is provided by the reconfigurable interface and the operation of the reconfigurable interface is defined by non-volatile on-chip memory. Therefore, Applicants respectfully request withdrawal of

the 35 U.S.C. §103(a) rejection with respect to Claims 1-6.

Applicants have now made an earnest attempt in order to place this case in condition for allowance. For the reasons stated above, Applicants respectfully request full allowance of the claims as amended. Please charge any additional fees or deficiencies in fees or credit any overpayment to Deposit Account No. 20-0780/CYGL-25,768 of HOWISON & ARNOTT, L.L.P.

Respectfully submitted,
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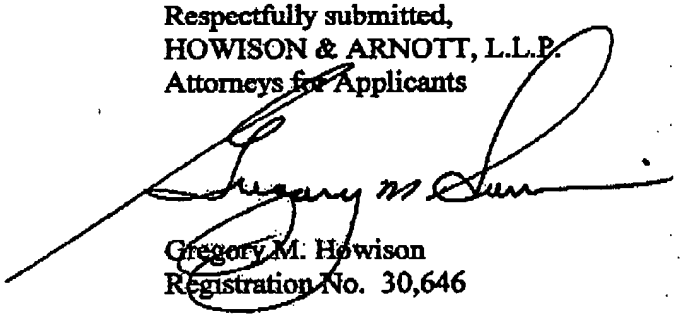

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